Enrollment No: _____ Exam Seat No:_____

C.U.SHAH UNIVERSITY

Summer Examination-2018

Subject Name : Digital Circuits

Subject Code : 4TE03DCI1 **Branch: B.Tech (Electrical)**

Semester : 3 **Date : 26/03/2018** **Time : 02:30 To 05:30** **Marks : 70**

Instructions:

(1) Use of Programmable calculator & any other electronic instrument is prohibited.
(2) Instructions written on main answer book are strictly to be obeyed.
(3) Draw neat diagrams and figures (if necessary) at right places.
(4) Assume suitable data if needed.

Q-1 **Attempt the following questions:** **(14)**

a) The NAND gate output will be low if the two inputs are 01
(A) 00 (B) 01
(C) 10 (D) 11

b) What is the binary equivalent of the decimal number 368 01
(A) 101110000 (B) 110110000
(C) 111010000 (D) 111100000

c) The decimal equivalent of hex number 1A53 is 01
(A) 6793 (B) 6739
(C) 6973 (D) 6379

d) $(734)_8 = (\_\_\_)_{16}$ 01
(A) C 1 D (B) D C 1
(C) 1 C D (D) 1 D C

e) The number of control lines for a 8– to –1 multiplexer is 01
(A) 2 (B) 3
(C) 4 (D) 5

f) How many Flip-Flops are required for mod–16 counter? 01
(A) 5 (B) 6
(C) 3 (D) 4

g) EPROM contents can be erased by exposing it to 01
(A) Ultraviolet rays. (B) Infrared rays.
(C) Burst of microwaves. (D) Intense heat radiations.

h) The hexadecimal number ‘A0’ has the decimal value equivalent to 01
(A) 80 (B) 256
(C) 100 (D) 160

i) The digital logic family which has minimum power dissipation is
(A) TTL (B) RTL 01
(C) DTL (D) CMOS

j) The output of a logic gate is 1 when all its inputs are at logic 0. the gate is either
(A) a NAND or an EX-OR (B) an OR or an EX-NOR 01
(C) an AND or an EX-OR (D) a NOR or an EX-NOR

k) The speed of conversion is maximum in
(A) Successive-approximation A/D converter. (B) Parallel-comparative A/D converter. 01
(C) Counter ramp A/D converter. (D) Dual-slope A/D converter.

l) The 2's complement of the number 1101101 is
(A) 0101110 (B) 0111110 01
(C) 0110010 (D) 0010011

m) When simplified with Boolean Algebra $(x + y)(x + z)$ simplifies to
(A) x (B) $x + x(y + z)$ 01
(C) $x(1 + yz)$ (D) $x + yz$

n) The gates required to build a half adder are
(A) EX-OR gate and NOR gate (B) EX-OR gate and OR gate 01
(C) EX-OR gate and AND gate (D) Four NAND gates.

Attempt any four questions from Q-2 to Q-8

Q-2 Attempt all questions **(14)**

a) Simplify: a) Y= (A+C)(A+D)(B+C)(B+D) 07
b) Y= (B+BC)(B+B'C)(B+D)

b) What is meant by multiplexer? Explain with diagram and truth table for the Operation of 4-to-1 line multiplexer. 07

Q-3 Attempt all questions **(14)**

a) Explain half and full adders in detail. 07

b) Explain the working of the Master Slave J K flip-flop with necessary logic diagram. 07

Q-4 Attempt all questions **(14)**

a) What is meant by decoder? Explain 3-to-8 line decoder with diagram and truth table. 07

b) With neat diagram explain the operation of 4- bit serial- in-serial –out register. Draw the timing diagram and give its truth table. 07

Q-5 Attempt all questions **(14)**

a) Explain the working of 4 bit asynchronous up counter. 07

b) Simplify with K- Map $F(w, x, y, z) = \Sigma (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$ 07

Q-6 **Attempt all questions** **(14)**

a) Describe S-R flip-flop and its applications. 07

b) State and explain De Morgan's theorem with the use of logic gates. 07

Q-7 **Attempt all questions** **(14)**

a) Explain TTL logic families in detail. 07

b) Simplify with K- Map in SOP and POS: $F(A, B, C, D) = \Sigma (0, 1, 2, 5, 8, 9, 10)$ 07

Q-8 **Attempt all questions** **(14)**

a) Which gates are known as Universal Gates? Justify them as Universal gates with the help of circuit diagrams and truth tables. 07

b) Write a technical note on Johnson counter. 07